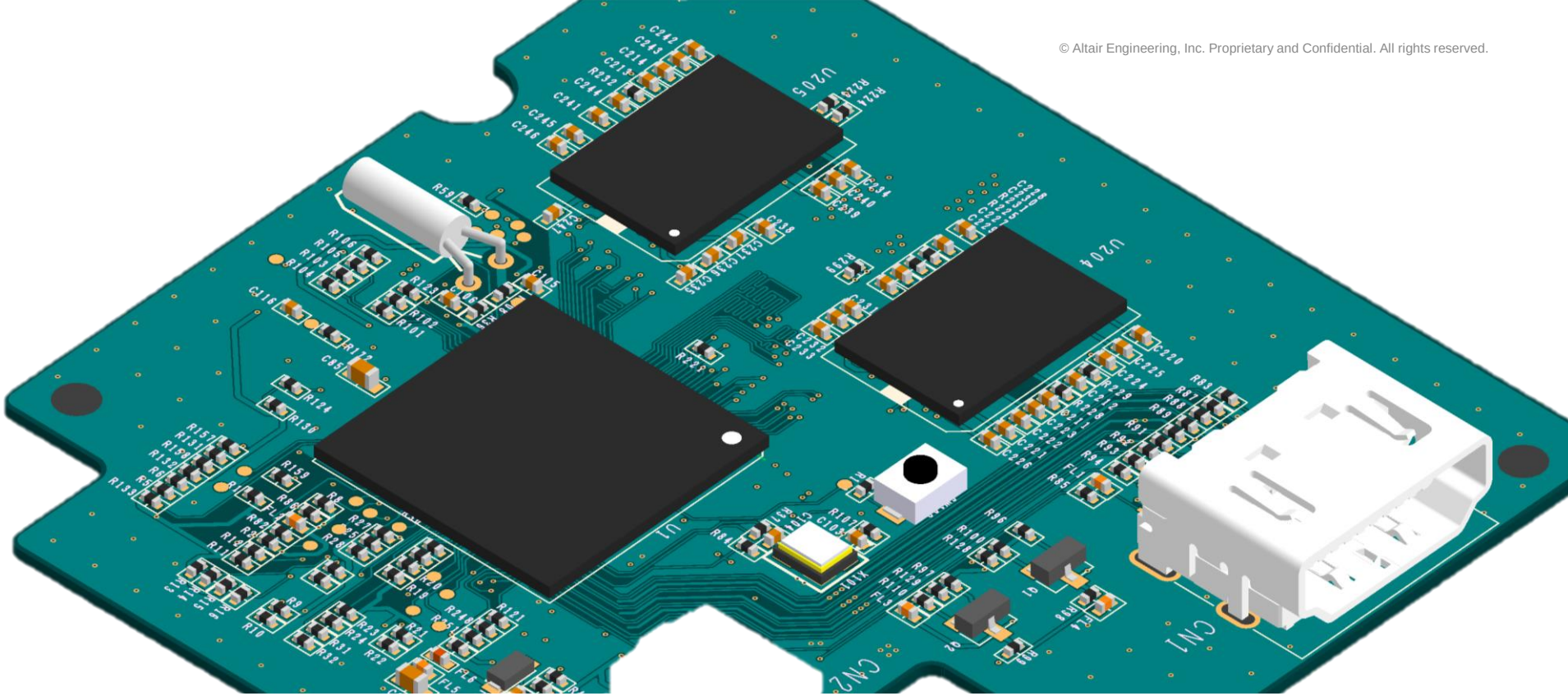
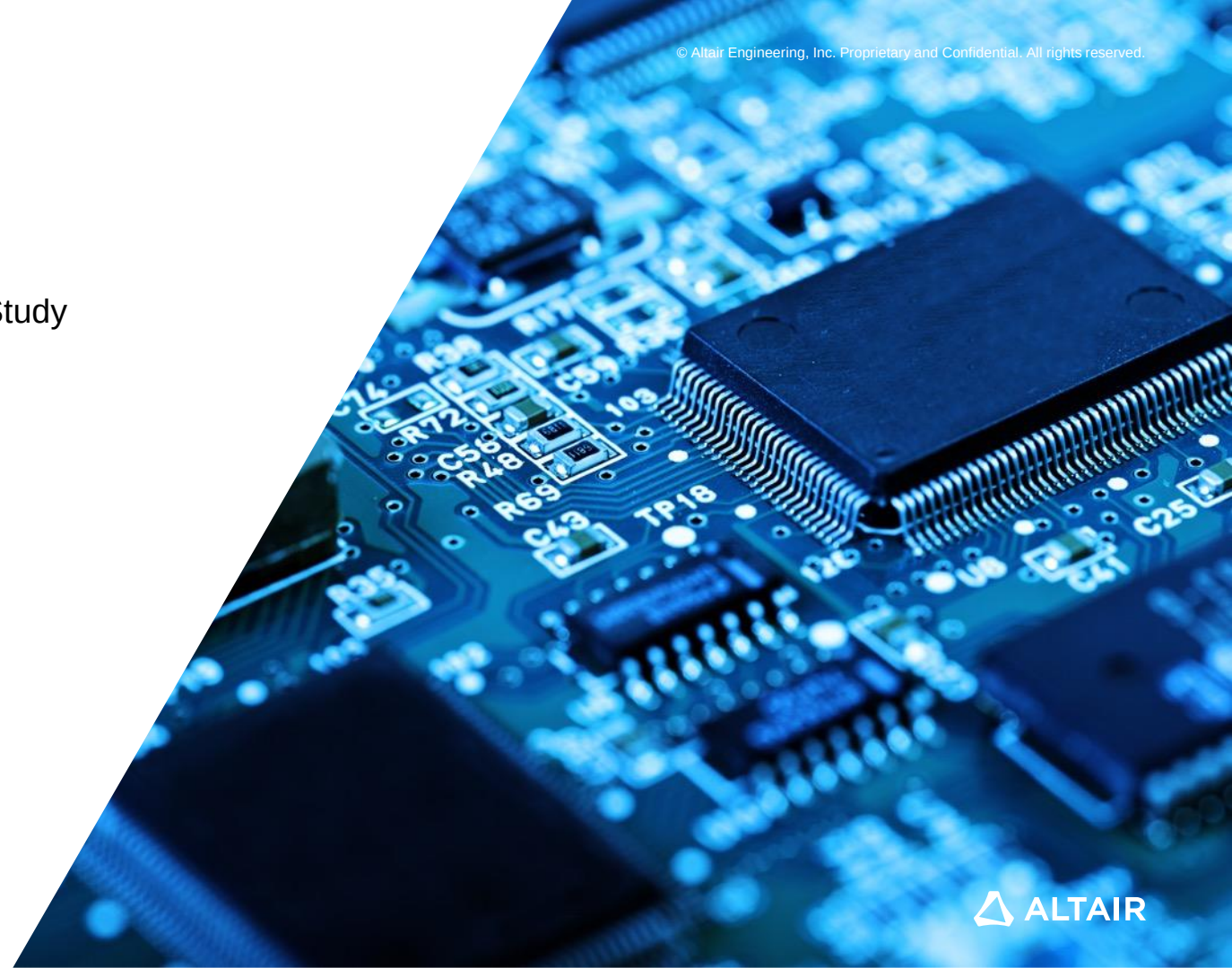


SIGNAL INTEGRITY ANALYSIS WITH ALTAIR POLLEX™ DDR DESIGN CASE

DaiHo Ham (daiho@altair.com), Dr Jordi Soler (jsoler@altair.com) – Sept 25, 2020

Outline

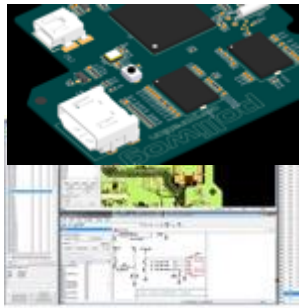
1. Introduction
2. DDR Design Case Study
3. Benchmark study
4. Summary



ALTAIR

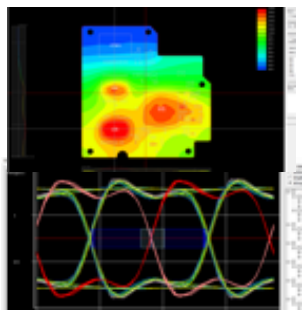
1. Altair PollEx

Altair PollEx is a PCB level EDA software suite available under Altair Units covering PCB design review, verification, analysis and manufacturing, to significantly reduce development cycles while providing a common application for schematic engineers, PCB designers, CAE analysts and manufacturing engineers to communicate



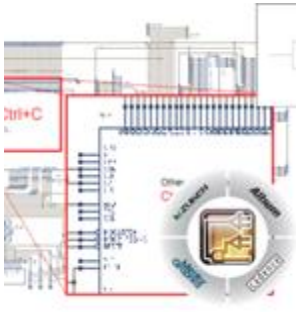
PCB Modeler with ECAD Connectivity

PCB Verification (DFE, DFM, DFA)

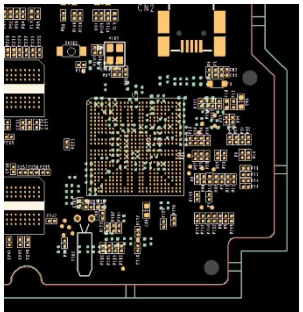


PCB Solvers (SI / PI / Thermal)

Unified Part Editor



Logic / CAM



Manufacturing

1. Altair Pollex Customer Base

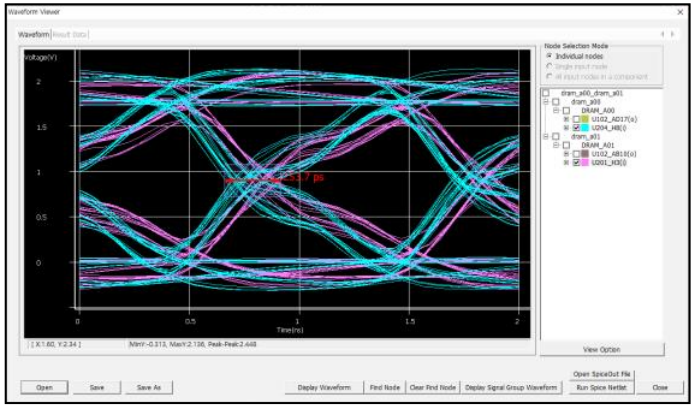
- Strong customer base with global customers and a leading position in South Korea
- Leading players with top level e-manufacturing technologies, including Samsung and LG, using PollEx

1. Introduction

PollEx Signal Integrity (SI)

The goal of SI in PollEx is to obtain the best signal quality by analyzing and adjusting multiple factors, including:

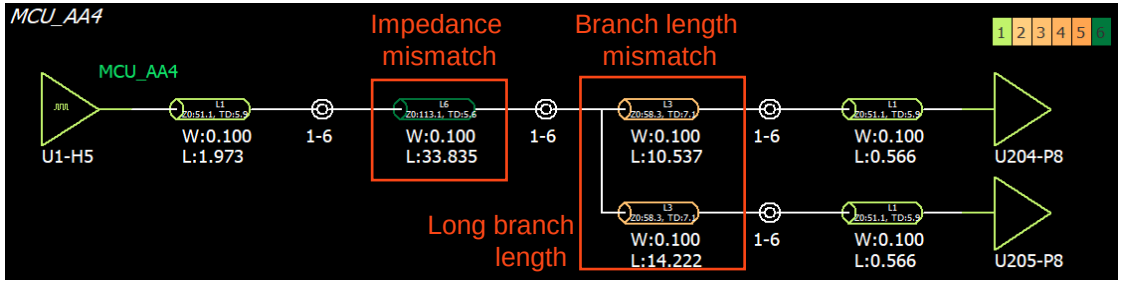
- Reflection due to impedance discontinuity, crosstalk, jitter due to Inter Symbol Interference (ISI)
- SI power and ground bounces, trace and via stubs, trace cross over plane split, improper signal return path, transmission line loss, improper net topologies
- Differential pair length mismatch , power distribution network problem, via parasitic, bus nets length mismatch, line delay difference between M/S and S/L structure, driver fan in/out, signal edge rate, trace self resonance, part to part skew

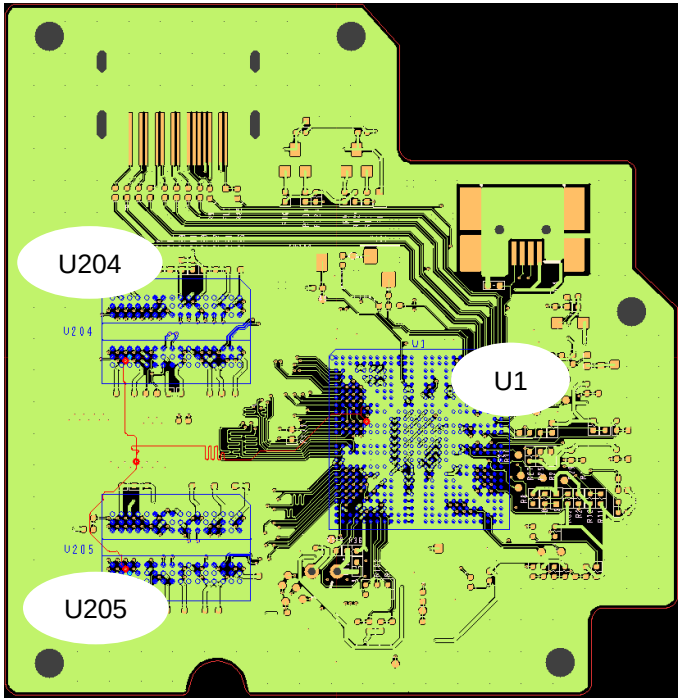


2. DDR Design Case Study

Description

- CPU (U1) drives signal into two memories (U204, U205)
- Operating Speed: DDR3_1066 AC175
- Drive strength: 30 mA
- Termination: None
- Topology: Tree topology (unbalanced and distributed)
- Impedance: Mismatched



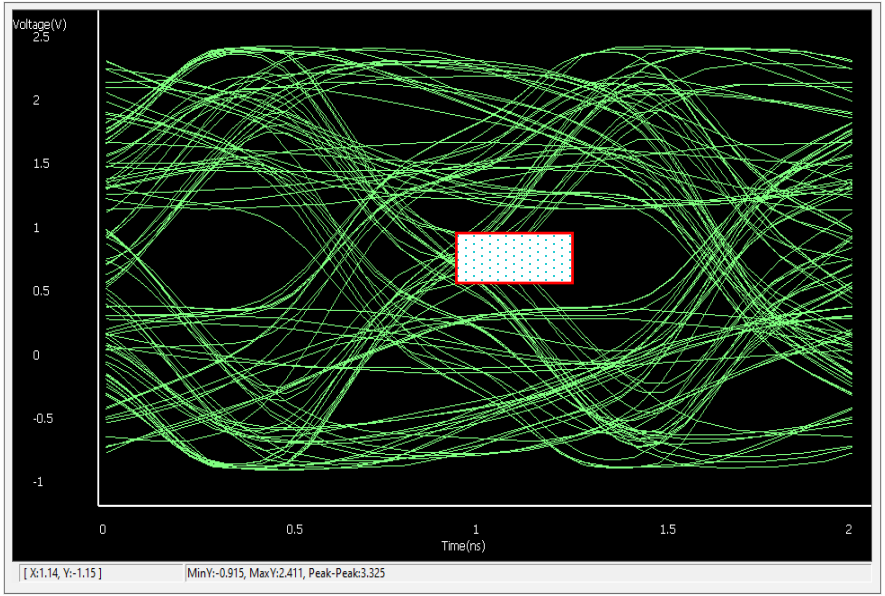


ALTAIR

2. DDR Design Case Study

Problem to Solve

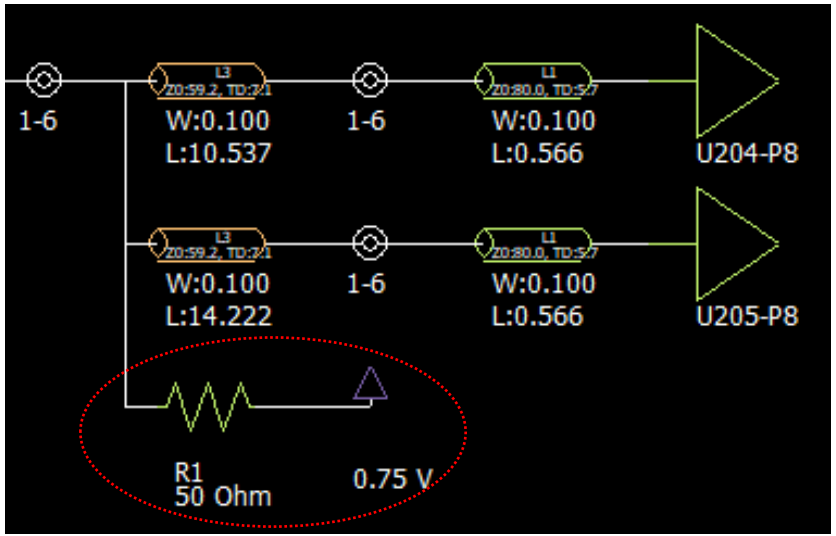
- The “Eye” is closed, and thus data communication is not possible
  - Overshoot / ringback is large due to the reflection noise caused by the impedance discontinuity
  - Timing skew exists between two memories caused by the unbalanced branch length.
  - Big jitter due to the Inter Symbol Interference (ISI)
  - Possibility that the ringback will be larger due to crosstalk or power noise.
  - The branch length is long, so it works as a distributed load.



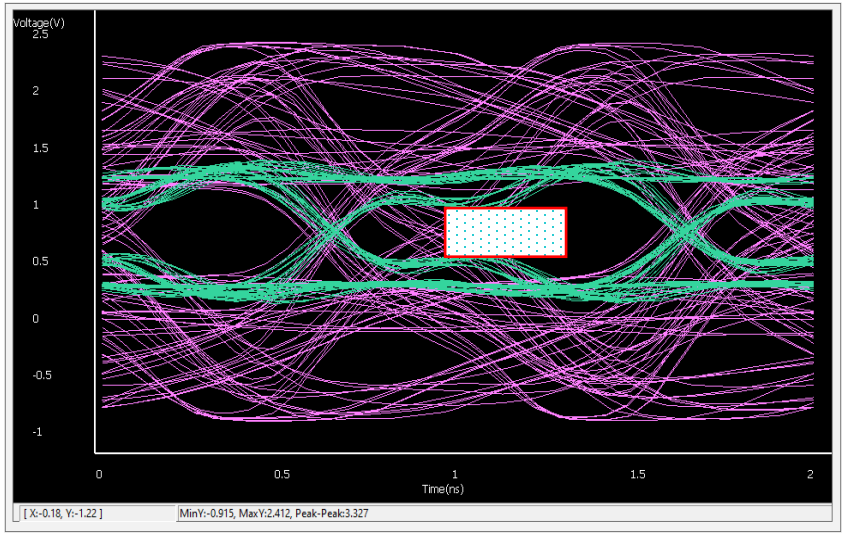
2. DDR Design Case Study

Improvement 1

Improvement - Added Thevenin type termination to reinforce impedance mismatch problem



Results - Decreased overshoot and opened Eye. However, the cyan colored improved waveform still touches the eye-mask

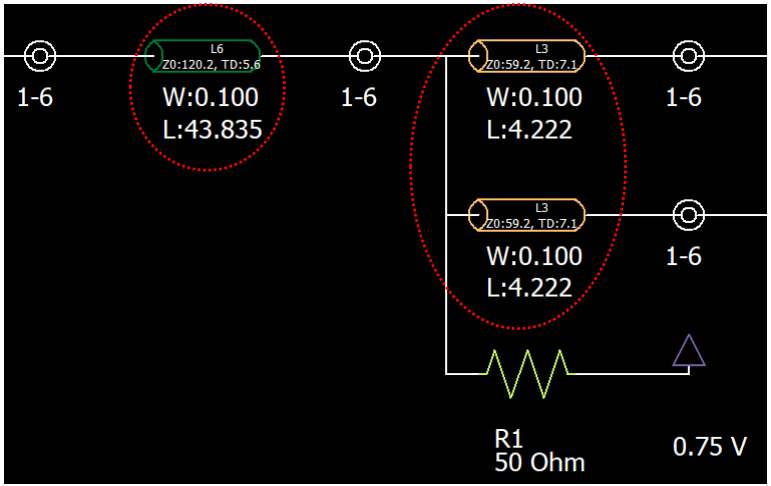


ALTAIR

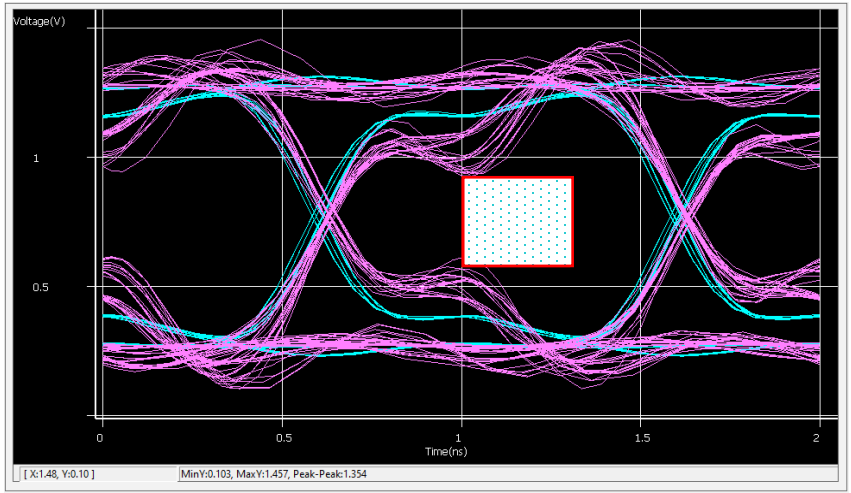
2. DDR Design Case Study

Improvement 2

Improvement - Adjusted to the same branch length of loads and changed to lumped load topology



Results - Improved voltage / timing margin (cyan-colored waveform)



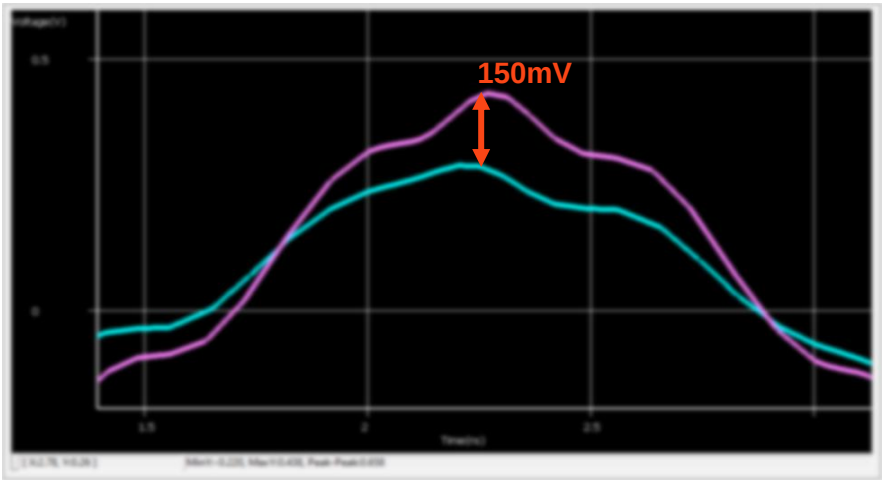
ALTAIR

2. DDR Design Case Study

Improvements 3

Improvement - Modified the layer stack up to reduce the gaps between the net and the reference plane

Results - Reduced FEXT amplitude (cyan-colored waveform)

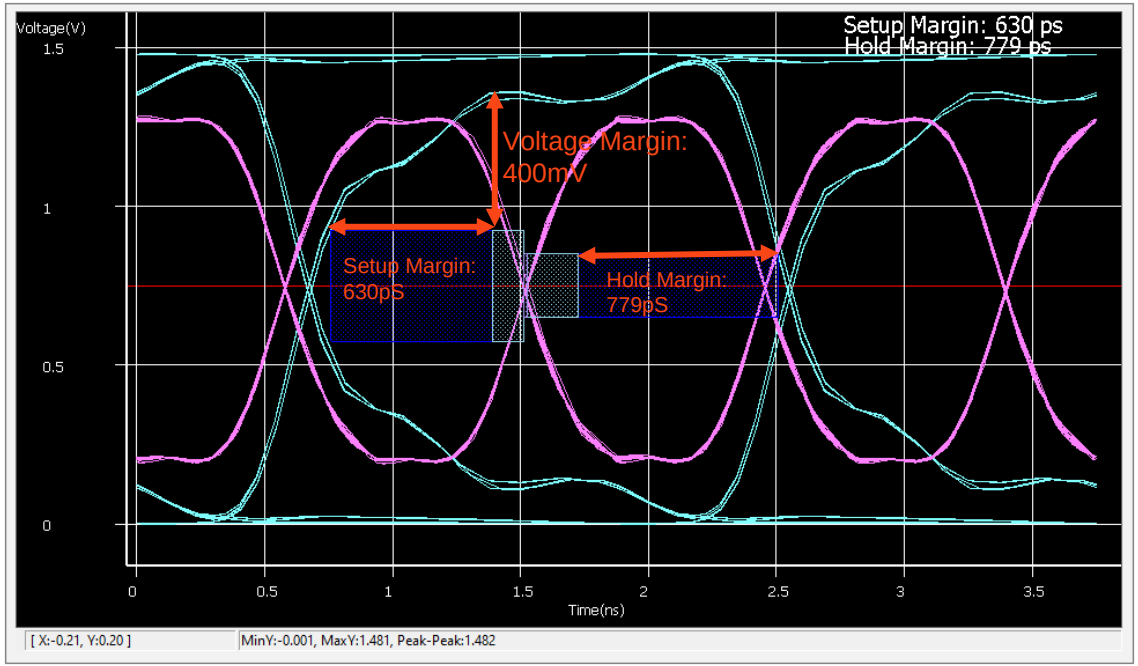


ALTAIR

2. DDR Design Case Study

Results

- Significant improvements in the design by applying the three changes
- Improved voltage margin up to 400mV and timing margin up to 630pS/779pS (setup / hold)

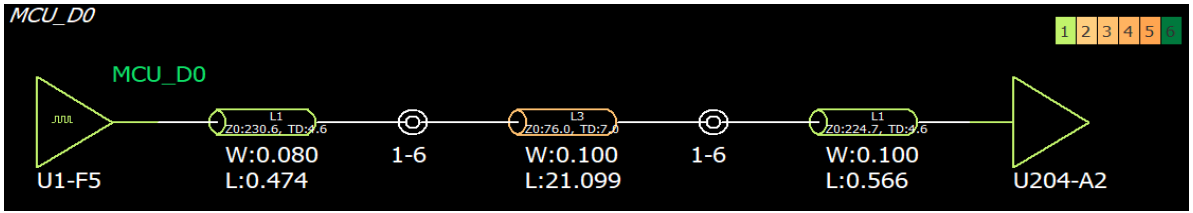


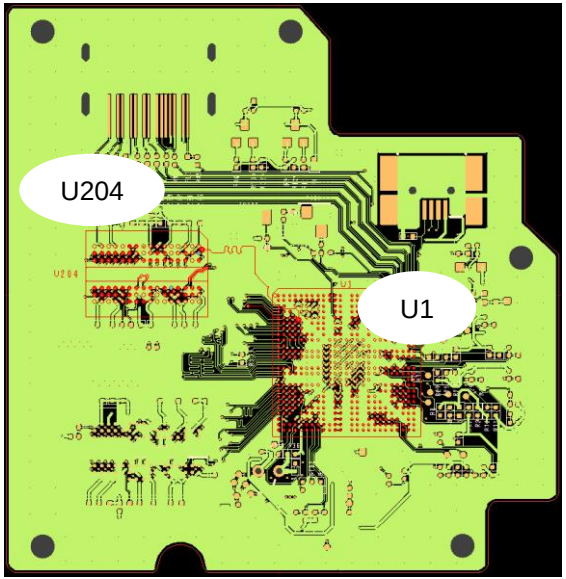
ALTAIR

2. Benchmark study

Single-Ended Case - Description

- CPU(U1) drives signal into memory (U204)
- Operating speed: DDR3_1066 AC175
- Drive strength: 60Ω (17.4 mA)
- Receiver termination: 120Ω Thevenin
- Topology: Point to point topology
- Ground condition: Ideal ground
- Bit Pattern: Periodic

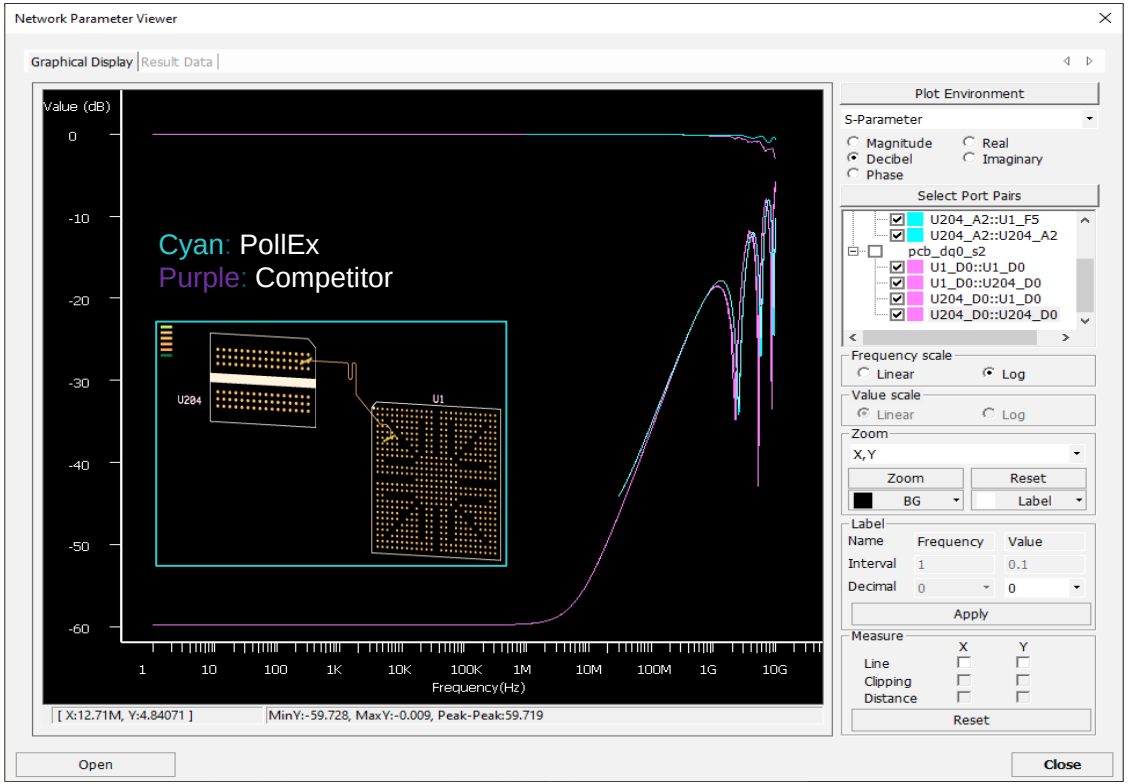




ALTAIR

3. Benchmark study

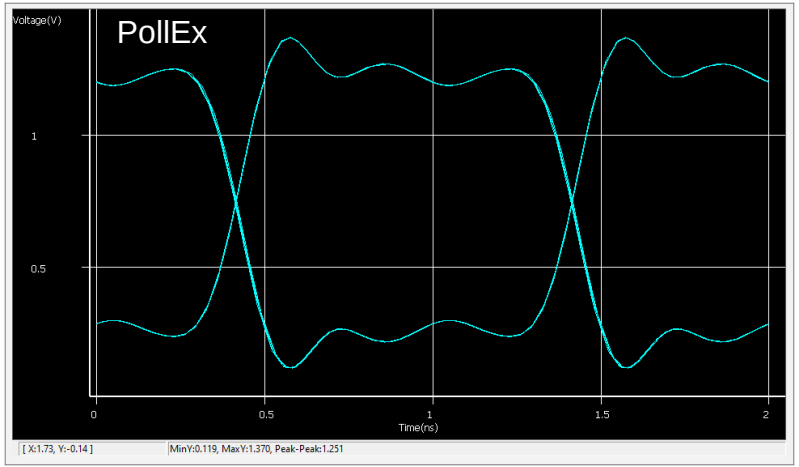
Single-Ended Case – S Parameters Results

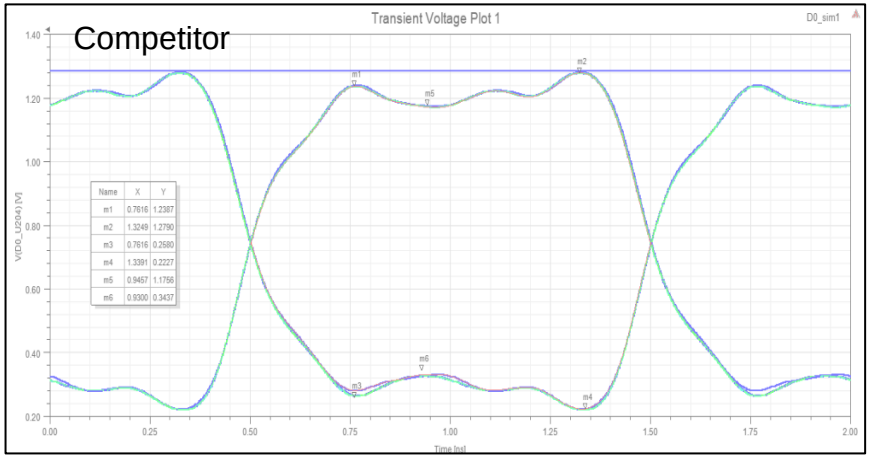


- Resonant frequencies are identical
- Amplitude at resonant point is slightly different but being this difference acceptable

3. Benchmark study

Single-Ended Case – Eye Diagram and Waveform Results





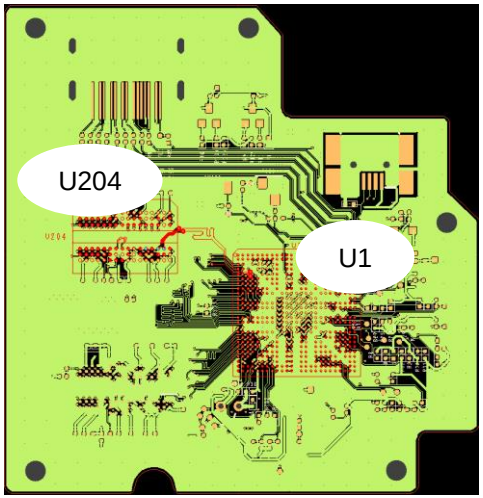
- Overshoot / ringback positions and quantities are identical
- The amplitude at each point is slightly different, but since the trend of the signal waveform is consistent, this degree of error can be tolerated

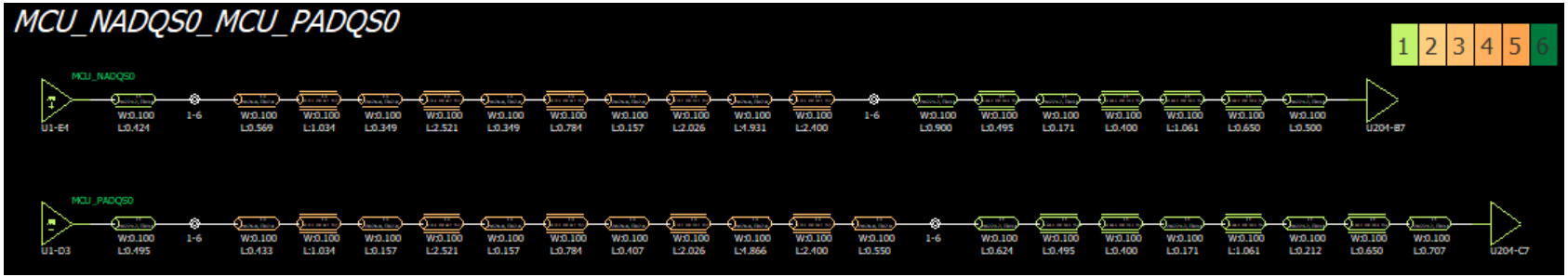
ALTAIR

3. Benchmark study :

Differential Line Case – Description

- CPU(U1) drives differential signal into memory (U204)
- Operating speed: DDR3_1066 AC175
- Drive strength: 60Ω (17.4 mA)
- Receiver termination: 120Ω
- Topology: Point to point
- Ideal ground
- Bit pattern: Periodic

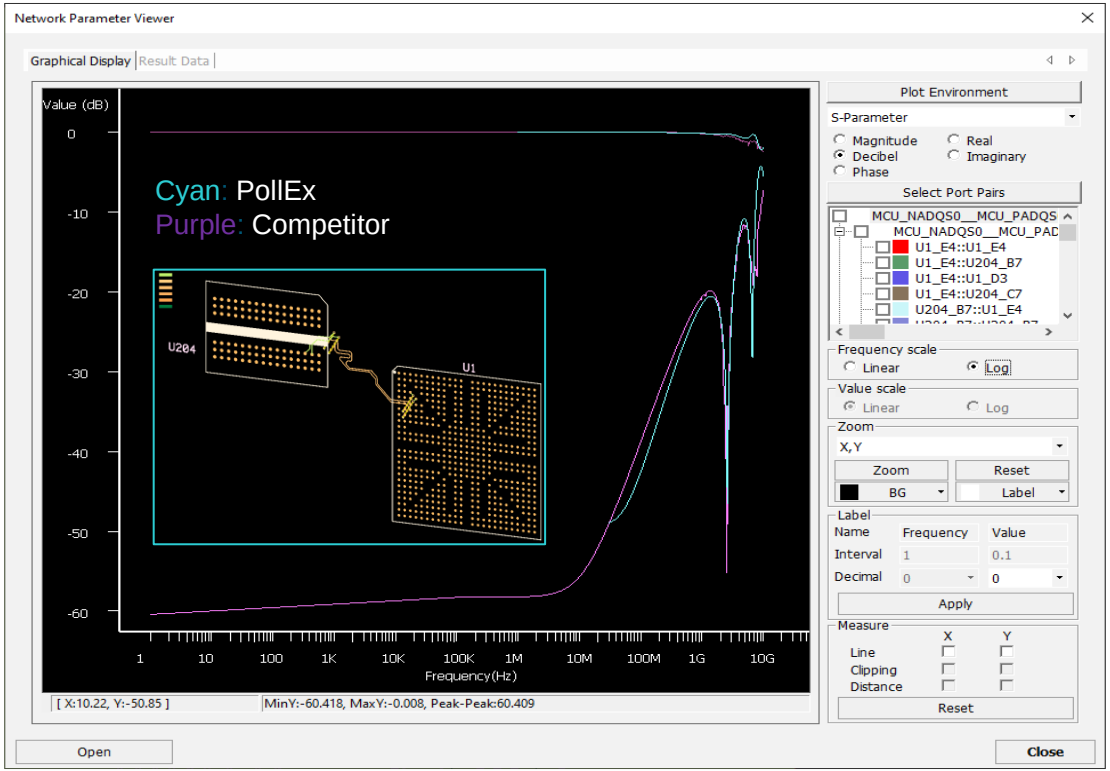




ALTAIR

3. Benchmark study

Differential Line Case – S Parameters Results

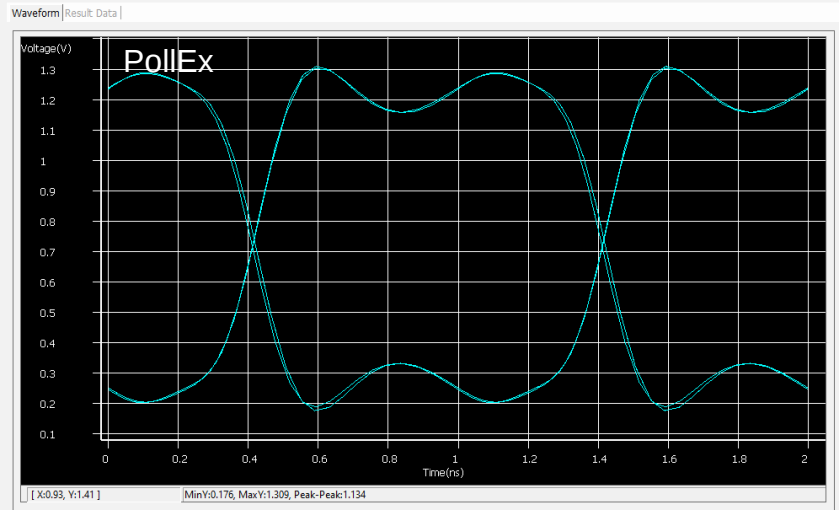


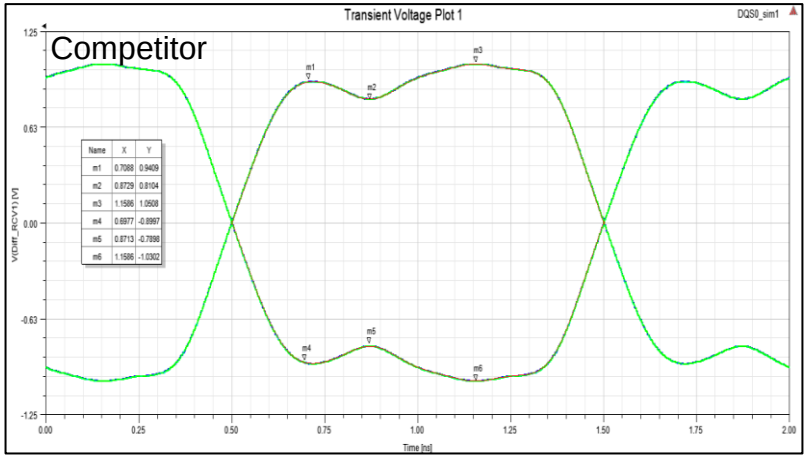
- Resonant frequencies are identical
- Amplitude at resonant point is slightly different but being this difference acceptable

ALTAIR

3. Benchmark study

Differential Line Case – Eye Diagram and Waveform Results





- Overshoot / ringback positions and quantities are identical
- The amplitude at each point is slightly different, but since the trend of the signal waveform is consistent, this degree of error can be tolerated

ALTAIR

4. Summary

- The purpose of SI applied in early development stages is to predict signal distortion when the driver waveform reaches the receiver stage and to secure the timing and voltage margins
- We have presented a DDR design case, where the overshoot caused by impedance mismatch is large, shortening the life of the IC and creating a large ringback, which can cause system malfunction when invading the threshold area
- Enough design margins with the elements which can be controlled in advance should be provided to have a robust design where unpredictable factors that cannot be predicted do not case system failure. We have shown 3 improvements:
  - In order to reduce the overshoot caused by impedance mismatch, add the appropriate value termination
  - Adjust the topology to balance the load to minimize the effect of reflection noise skew
  - Crosstalk noise can worsen ringback, thus reduce crosstalk noise as much as possible
- Being fast and reliable, PollEx SI provides the same level of accuracy as a competing and long-established SI EDA analysis software

THANK YOU

altair.com/pollex

#ONLYFORWARD

ALTAIR